FIG. 3 of Matsunaga is a sectional view of the semiconductor device illustrated in FIG. 2 on which a bonding wire is formed. FIGS. 2 and 3 are shown below.

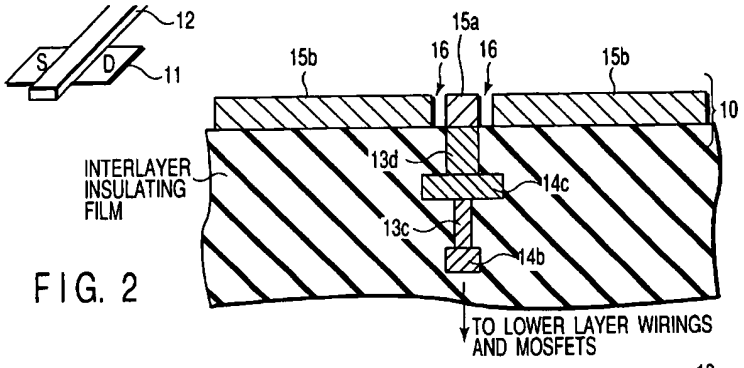


FIG. 2

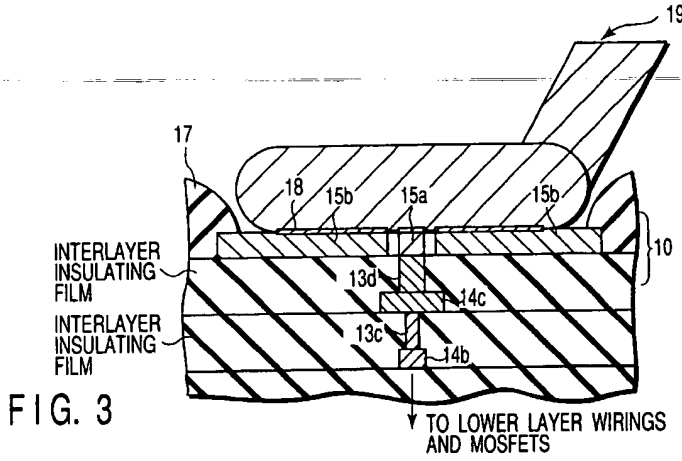


FIG. 3

Referring to FIG. 2, Matsunaga describes the *pad electrode 10* of the device as being made of split *pad electrodes 15a, 15b* (cols. 5-6, bridging paragraph, and col. 6, lines 46-53). The pad electrode 15a is disposed in the center and surrounded by the pad electrode 15b, which is a floating electrode and not connected to any wirings. See at col. 5, line 51 to col. 6, line 9 (emphasis added):

> As shown in FIG. 1 and FIG. 2, ...connected to a first split pad electrode 15a of a pad electrode 10 ...A second split pad electrode 15b of the pad electrode 10 is disposed with a clearance 16 near the film thickness (for example, 1 μm) of the pad electrode 10 to the first split pad electrode 15a so as to surround the first split pad electrode 15a.
>
> Here, the first split pad electrode 15a is, for example, a 2 μm by 2 μm square. The second split pad electrode 15b is, for example, a 100 μm by 100 μm square with void inside.
>
> As outlined above, the pad electrode 10 used in the present invention comprises the first split pad electrode 15a disposed in the center and the second split pad electrode 15b disposed apart

from the first split pad electrode 15a so as to surround the first split pad electrode 15a. The first split pad electrode 15a is connected to the wirings...whereas the second split pad electrode 15b is not connected to the wirings...in the semiconductor device. Namely, the second split pad electrode 15b is made to be a floating electrode.

As described in Matsunaga and illustrated in FIG. 2, the pad electrodes 15a, 15b are *single* layers.

Contrary to the Examiner's assertion, layer 18 is *not* part of either of the pad electrodes 15a, 15b. As illustrated in FIG. 3, layer 18 is an alloy layer applied to the pad electrodes 15a, 15b for the purpose of bonding the bonding wire 19 onto the pad electrodes 15a, 15b. See at col. 6, lines 10-17 (emphasis added):

> FIG. 3 is a sectional view showing the condition of the semiconductor device on which bonding to the pad electrode shown in FIG. 2 is conducted. As shown in FIG. 3, a part of the second split pad electrode 15b is covered with a passivation film 17. *A bonding wire 19 is bonded onto the first and second split pad electrodes 15a and 15b,* which are not covered with the passivation film 17, *through an alloy layer 18.*

This is further supported by the description by Matsunaga of probing the pad electrodes 15a. 15b for evaluation of the semiconductor device (at col. 6, lines 35-45, emphasis added), which is illustrated in FIG. 5 below.

> FIG. 5 shows a sectional view of the condition of the semiconductor device in which *probing is conducted on the pad electrode shown in FIG. 2.*
>
> In usual probing, a probe 22 slides on the pad electrode 10 and breaks a natural oxide film on the surface of a material (e.g., Al) of the pad electrode 10 and intrudes thereinto. By these breaking actions, *the first split pad electrode 15a is connected to the second split pad electrode 15b during probing as shown in FIG. 5.* Therefore, also in probing for the evaluation of the semiconductor device, electrical connection of the pad electrode 10 can be achieved sufficiently.

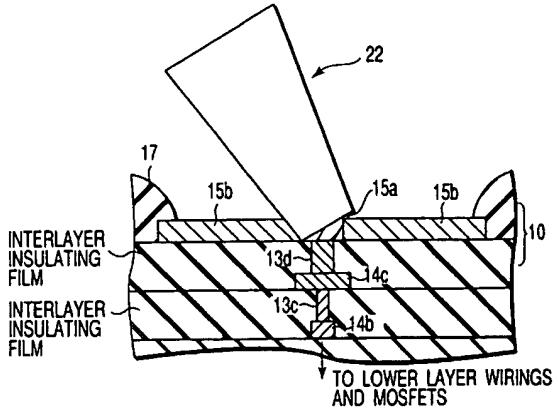


FIG. 5

Clearly, alloy layer 18 is *not* part of either of the pad electrodes 15a, 15b.

It is clear from the description and illustrations, particularly the illustrations of FIG. 2 and FIG. 5 that the pad electrodes of Matsunaga are a *single layer* and not two layers as disclosed and claimed by Applicant.

Matsunaga does not teach or suggest Applicant's bond pad structure as claimed. Accordingly, withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. § 102(e) (Sheu)

The Examiner rejected Claims 22, 24, 26, 27, 71 and 74 under Section 102(e) as anticipated by USP 6,455,943 (Sheu). This rejection is respectfully traversed.

The Examiner cites Sheu as disclosing all of the elements of the claims. The Examiner particular cites to FIG. 4 of Sheu, illustrated below.

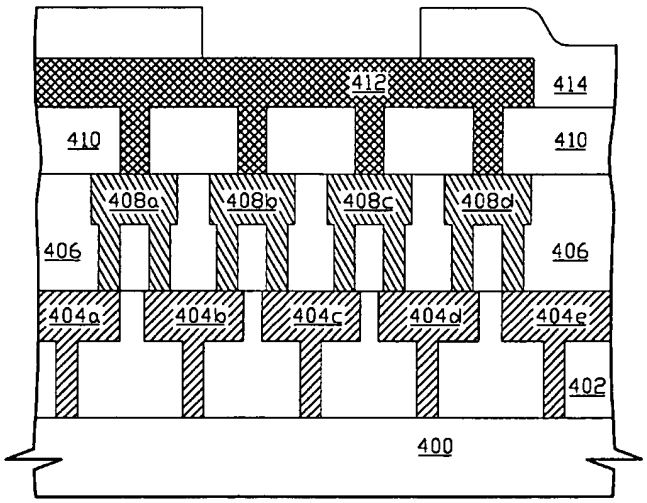


FIG.4

Sheu does not describe first and second bonding pads as claimed. Referring to FIG. 4, Sheu teaches a bonding pad structure made of conductive islands and plugs 404a-404e and 408a-408d and *a single bonding pad layer 412*. The islands and plugs are used to fasten the bonding pad layer 412 and prevent it from peeling or cracking during the wire bonding process. See at cols. 5-6, bridging paragraph (emphasis added):

> Referring to FIG. 4, still another bonding pad structure formed by using a dual damascene process is shown. The conductive islands and the conductive plugs are formed together. A substrate 400, dielectric layers 402, 406 and 410, *dual damascene structures 404a-404e and 408a-408d, **a bonding pad layer 412***, and a passivation layer 414 are shown in this figure. The dual damascene structures 404a-404e and 408a-408d are used to fasten the bonding pad layer 412 to prevent the bonding pad layer 412 from peeling or cracking....

The Examiner mischaracterizes the conductive islands and plugs 404a-404e and 408a-408d as "bonding pads" and further mischaracterizes the bonding pad layer 412 as a "conductive material" (with regard to Claims 24, 26, 27).

It is clear from the description and illustration of FIG. 4 that the bond pad structure of Sheu is a *single bond pad* 412 and not two bond pads as disclosed and claimed by Applicant.

Sheu does not teach or suggest Applicant's bond pad structure as claimed. Accordingly, withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. §103(a)

The Examiner rejected Claims 3, 4, 30, 33, 51 and 56 under Section 103(a) as obvious over Matsunaga in view of USP 6,078,100 (Duesman); Claims 6, 15, 20 and 54 as obvious over Matsunaga in view of USP 6,509,643 (Ohtaka); Claim 19 as obvious over Matsunaga; Claim 23 as obvious over Sheu in view of USP 5,883,435 (Geffken); and Claim 25 as obvious over Sheu in view of Ohtaka. These rejections are respectfully traversed.

As Matsunaga and Sheu are inapplicable for the above-stated reasons, combining the disclosures of any of the secondary references of Duesman, Ohtaka or Geffken does not obviate any of the claims.

Duesman describes the formation of routing traces on an external surface of a semiconductor device to connect portions of the internal circuitry of a die rather than forming

such routing traces internally. In other embodiments, the routing traces can be fabricated to connect two or more semiconductor dice, or for use as repair mechanisms.

Contrary to the Examiner's statement, elements 132A-132C are *internal traces* — <u>not</u> bonding pads. Internal traces 132 are illustrated in FIG. 4a and described at col. 5, lines 35-45 as follows (emphasis added):

> The first routing trace 122 is an example of a short "jumping" trace. Referring to FIGS. 4a-4b, the path for connecting ***first internal trace 132*** with second internal trace 134 is blocked by a lateral trace 136 which is running perpendicular to the plane of the cross-section on a fourth level 138 of the multilevel structure of the flip-chip 100. A first internal trace-to-first trace contact 142 is formed to connect the *first internal trace 132* with the first routing trace 122 and a first trace-to-second internal trace contact 144 is formed to connect the first routing trace 122 with the second internal trace 134, thereby "jumping" the lateral trace 136.

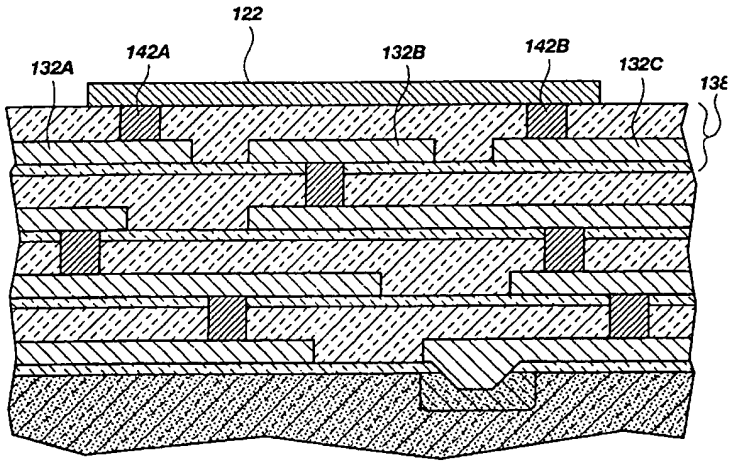


Fig. 4a

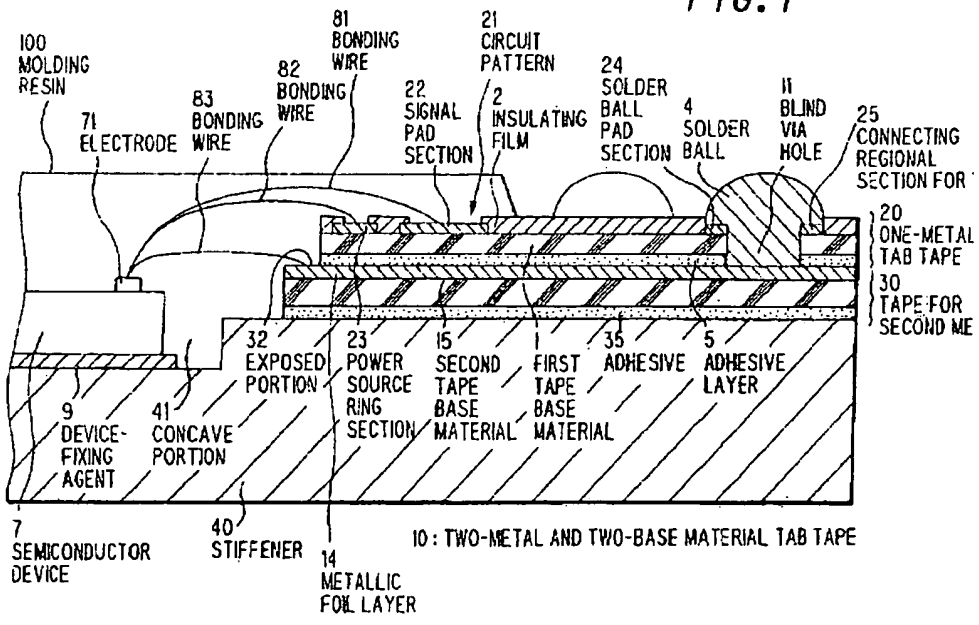
FIG. 4a does not illustrate bond pads. The Examiner has mischaracterized the *internal traces* 132 in Duesman as "bond pads." The combination of Duesman with Matsunaga does not obviate Claims 3, 4, 30, 33, 51 and 56. Accordingly, withdrawal of this rejection is respectfully requested.

Ohtaka describes a semiconductor device composed of a TAB tape with a stiffener. The Examiner contends that Claims 6, 15, 20 and 54 are made obvious by the substitution of Ohtaka's disclosure in FIG. 1 of a solder ball 4 for Matsunaga's "conductive material."

First of all, Ohtaka does not teach or suggest the placement of a conductive material (e.g., solder material) to interconnect two bond pads. Rather, Ohtaka describes mounting a solder ball 4 in a via hole 11 in contact with a metallic foil layer 14. See FIG. 1, and Ohtaka at col. 7, lines 20-25, and cols. 7-8, bridging paragraph:

> FIG. 1 illustrates a structure wherein a solder ball 4 is molten to mount in a blind via hole 11 composed of a via hole 12 and an opening 13, whereby it becomes possible to afford a specific potential to a metallic foil layer 14 beneath a one-metal TAB tape 20, so that an electrical connection is made in the blind via hole 11.
>
> ...
>
> Moreover, a solder ball 4 is molten to mount in a blind via hole 11 composed of the above-described via hole 12 and an opening 13, whereby an electrical connection is made between a connecting regional section 25 used for a via in the upper edge of the hole and a part of a metallic foil layer 14 in the bottom of the hole, so that a specific ground potential is afforded to the metallic foil layer 14 situated beneath a one-metal TAB tape 20. As a result, it becomes possible to suppress generation of noise due to electromagnetic field coupling between leads in a circuit pattern 21 on either surface of a one-metal TAB tape and to achieve speeding up of a velocity of propagation.

FIG. 1



Ohtaka does not teach or suggest interconnecting two bond pads with a conductive material.

Furthermore, as stated above, Matsunaga teaches pad electrodes 15a, 15b that are each a *single layer* — not two layers as claimed by Applicant. Accordingly, even if, *arguendo*, one were to utilize a solder material based on Ohtaka to connect the pad electrodes 15a, 15b of Matsunaga, this would not arrive at Applicant's device as recited in Claims 6, 15, 20 and 54. Accordingly, withdrawal of this rejection is respectfully requested.

Regarding the rejection of Claim 19, the Examiner maintains that it would be obvious to rearrange the passivation layer in Matsunaga's structure to overlie a portion of each of the bond pads.

As discussed above, Matsunaga teaches a structure whereby a pad electrode 15a is disposed *in the center and surrounded by* pad electrode 15b. See, for example, FIG. 1 showing pad 15a disposed within pad 15b.

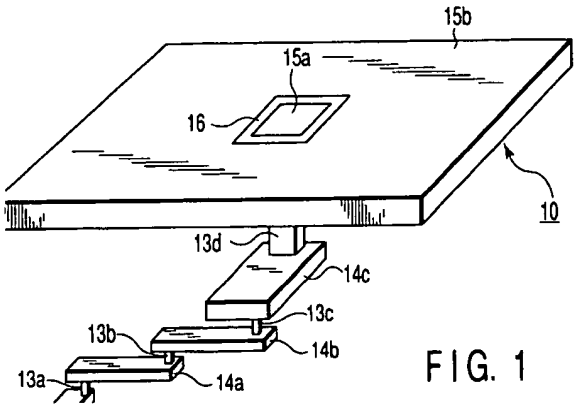


FIG. 1

Matsunaga addresses the application of a passivation layer over the pad electrodes, and essentially *teaches away* from applying a passivation layer over a portion of pad electrode 15a. See at col. 6, line 65 to col. 7, line 39 (emphasis added):

> In the meantime, generally, when a pad electrode is split, a clearance is formed between the split pad electrodes and the side surface of the split pad electrode is exposed. If this side surface is brought into contact directly with a resin for sealing a semiconductor device, there is the case where the pad electrode is corroded from the exposed side surface of the pad electrode by, for

example, the interaction between the water intruded from the outside through this resin and ionic impurities in the resin. *For this, in order to prevent the corrosion of the exposed side surface of the pad electrode,* ***there is the idea that the clearance between the split pad electrodes is covered with a passivation film.*** *In this case, the surface of each of the split pad electrodes is exposed from each different opening formed in the passivation film.* ***However, the passivation film covering the clearance is sometimes broken during bonding and its residue causes the durability during bonding to be impaired.***

In the first embodiment, on the other hand, as to the condition after the bonding is finished as shown in FIG. 3 and FIG. 4, bonding can be carried out such that the contact surface between both the bonding wire and the bump and the pad electrode 10 surrounds the inner periphery of the second split pad electrode 15b disposed so as to surround the island-like first split pad electrode 15a. Therefore, the clearance 16 between the first split pad electrode 15a and the second split pad electrode 15b *can be completely covered with the bonding wire and the bump and the side surface of each of the first and second split pad electrodes 15a and 15b is not exposed.* The surface of each of the first and second split pad electrodes 15a and 15b is exposed from one opening of the passivation film 17 covering the peripheral part of the second split pad electrode 15b ***and the passivation film is not formed so as to cover the clearance splitting the pad electrode and this makes it possible to be free from the problem that the durability during bonding is impaired.*** Also, to prevent the corrosion of the pad electrode from the clearance between the split pad electrodes as aforementioned, it is more preferable that the clearance between the first split pad electrode and the second split pad electrode be filled with an insulating film by using a damascene structure shown in a second embodiment explained later.

There is nothing in Matsunaga that would motivate one skilled in the art to fabricate a passivation to overlie each of the pad electrodes 15a, 15b.

Furthermore, as stated above, Matsunaga teaches pad electrodes 15a, 15b that are each a *single layer* — not two layers as claimed by Applicant.

The disclosure of Matsunaga does not teach or suggest the bond pad structure recited in Claim 19. Accordingly, withdrawal of this rejection is respectfully requested.

With regard to Claim 23, the Examiner maintains that it would be obvious to modify Sheu's structure "by using the solder material for the passivation layer" based on the disclosure of Geffken. (It is assumed that the reference to "solder material" is a typographical error, and that the Examiner is asserting that it would be obvious to modify Sheu's structure with a passivation layer having an opening to expose the bond pads.)

Geffken discloses a semiconductor device having vias opened to landing lines and selectively opened to a portion of personalization lines through a dielectric layer.

Contrary to the Examiner's statement, Sheu *does* disclose a passivation layer formed over the single bond pad (412) with an opening exposing the bond pad. The Examiner is directed to FIG. 4 and Sheu's description at cols. 5-6, bridging paragraph.

> Referring to FIG. 4, still another bonding pad structure formed by using a dual damascene process is shown. The conductive islands and the conductive plugs are formed together. A substrate 400, dielectric layers 402, 406 and 410, dual damascene structures 404a-404e and 408a-408d, ***a bonding pad layer 412, and a passivation layer 414 are shown in this figure***...The *passivation layer 414* can be a silicon dioxide layer or a silicon nitride layer formed by a conventional chemical vapor deposition process.

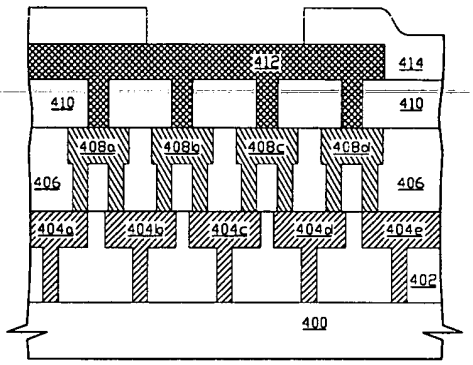


FIG.4

Furthermore, as stated above, Sheu teaches a *single bond pad* 412 — not two bond pads as claimed by Applicant.

The disclosure of Geffken combined with Sheu does not teach or suggest the bond pad structure recited in Claim 23. Accordingly, withdrawal of this rejection is respectfully requested.

As for Claim 25, the Examiner asserts that Sheu discloses all the elements of Claim 25 except for the conductive material comprising a solder material. However, the Examiner maintains that it would be obvious to modify Sheu's device by using a solder material for the conductive material based on the disclosure in Ohtaka.

Claim 25, depending from Claims 22 and 24, recites a conductive material comprising solder material interconnecting the first bond pad to the second bond pad.

First of all, as previously stated, Sheu teaches a *single bond pad* 412 — not two bond pads as claimed by Applicant. Furthermore, Sheu does not disclose interconnecting two bond pads with a conductive material. Nor does Ohtaka.

As discussed above, Ohtaka describes mounting a solder ball in a via hole in contact with a foil layer — not interconnecting two bond pads.

The disclosure of Ohtaka combined with that of Sheu does not teach or suggest the bond pad structure recited in Claim 25. Accordingly, withdrawal of this rejection is respectfully requested.

In sum, neither Matsunaga nor Sheu, either alone or combined with the secondary references of Duesman, Ohtaka or Geffken, teach or suggest Applicant's bond pad structure as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

Cited Prior Art. The prior art made of record and not relied upon is acknowledged. Nothing in those references teaches or suggests Applicant's bond pad structure as claimed.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine M. Strodthoff

Dated: MAY 28, 2003, 2003

Kristine M. Strodthoff
Reg. No. 34,259

WHYTE HIRSCHBOECK DUDEK S.C.
111 East Wisconsin Avenue, Suite 2100
Milwaukee, Wisconsin 53202
(414) 273-2100
Customer No. 31870